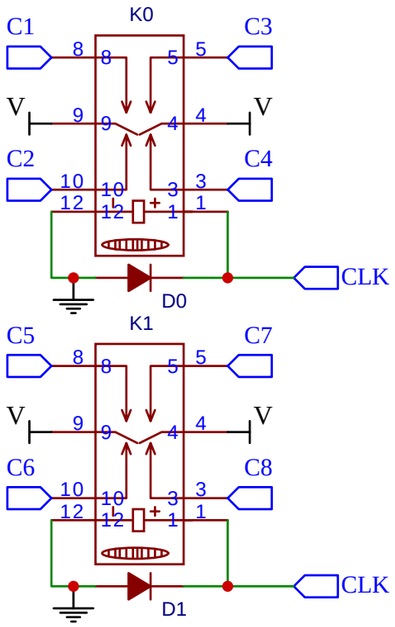
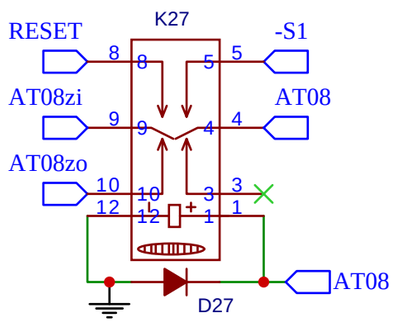
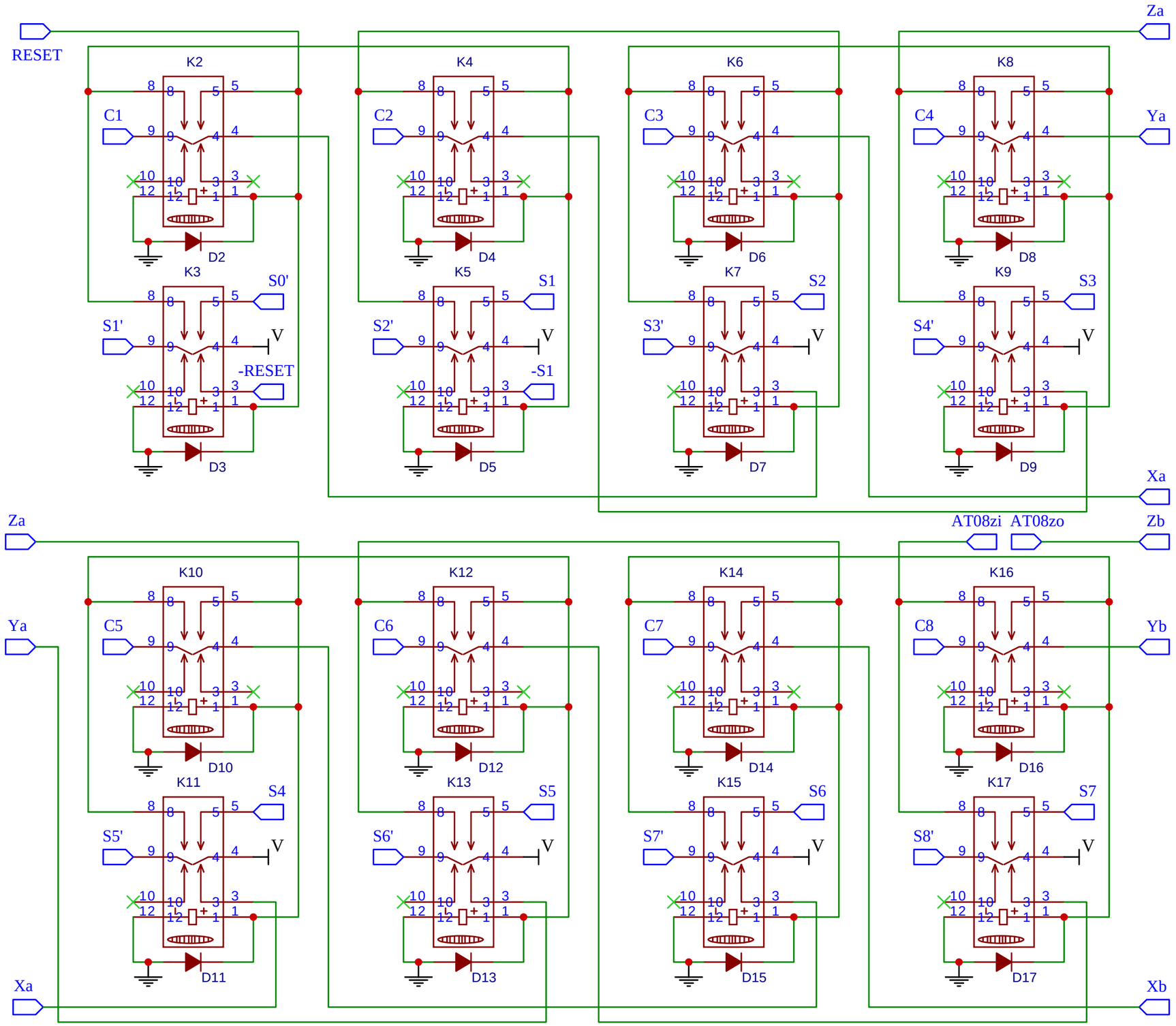
Sheet 1: 8 Stage FSM

Clock Divider



Abort Latch





CLK and RESET signals connect to control X bus (sheet 4)

AT08 signal connect to OP bus via upper card interconnect (sheet 4)

Xb, Yb, Zb connect to next FSM stage (sheet 2)

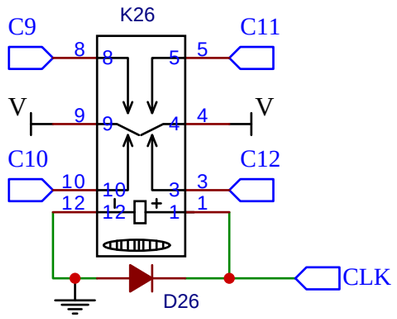
S1-S7, S0'-S8', ~S1 signals connect to next FSM stage, pulse distribution and indicators (sheet 2, 3 & 5)

TITLE: Relay Computer : Sequencer Lower Card	REV: 1.1
Company: Paul Law	Sheet: 1/5
Date: 2019-09-23 Drawn By: paul_6392	

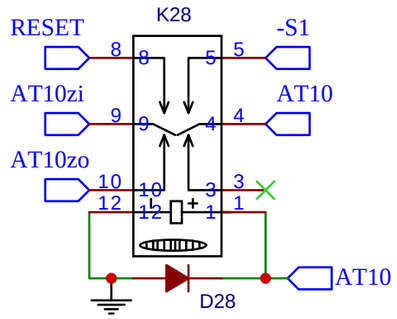
Relay Computer

Sheet 2: 10/12 Stage FSM

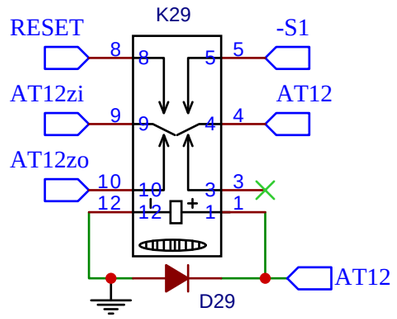
Clock Divider

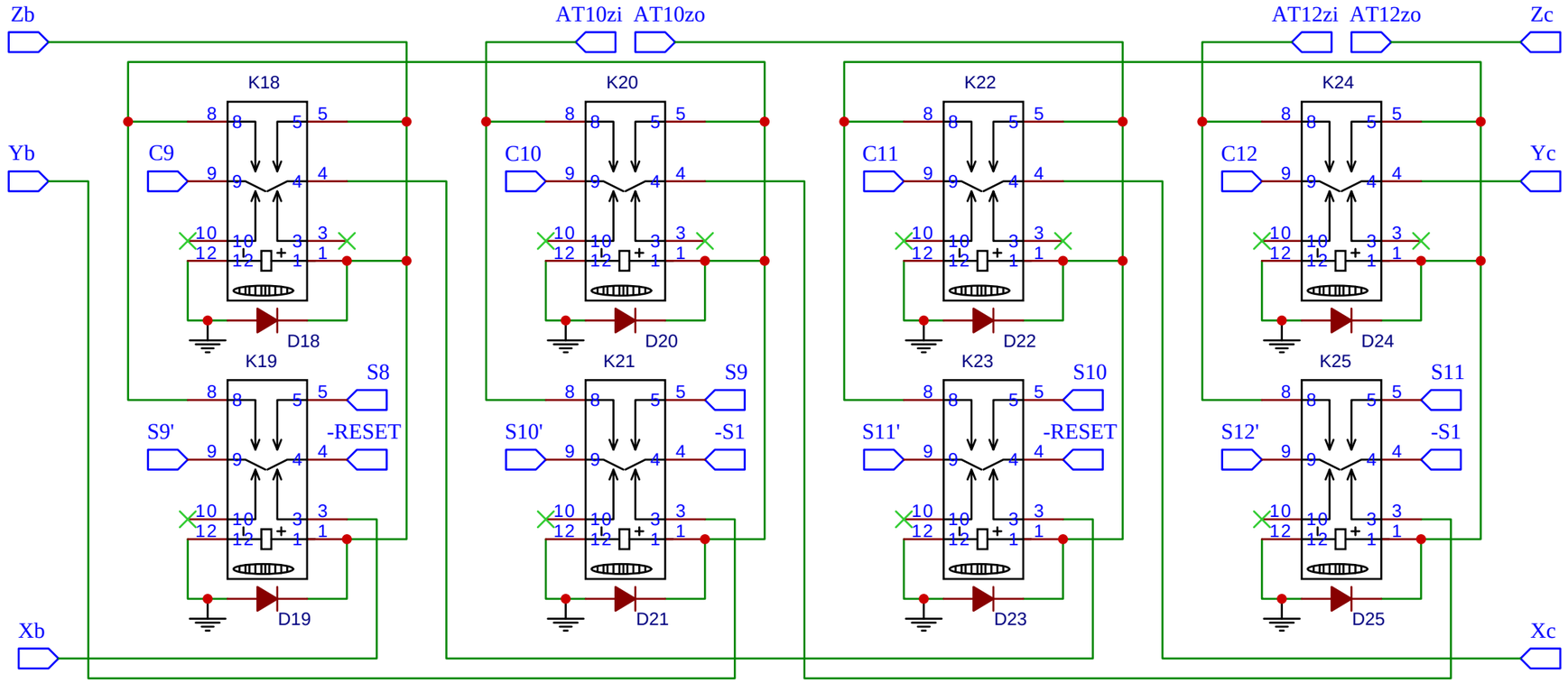


Abort Latch 10



Abort Latch 12





CLK and RESET signals connect to control X bus (sheet 4)

AT10 and AT12 signal connect to OP bus via upper card interconnect (sheet 4)

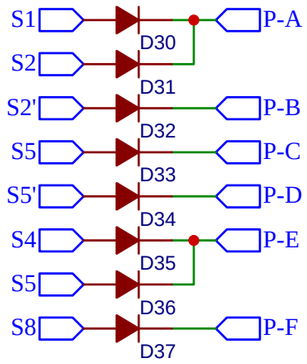
Xb, Yb, Zb connect from previous FSM stage (sheet 1)

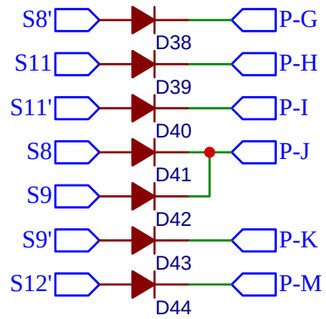
Xc, Yc, Zc connect to next FSM stage via upper card interconnect (sheet 4)

S8-S11, S9'-S12', ~S1 signals connect to prev FSM stage, pulse distribution and indicators (sheet 1, 3 & 5)

TITLE: Relay Computer : Sequencer Lower Card		REV: 1.1
RC Relay Computer	Company: Paul Law	Sheet: 2/5
	Date: 2019-09-23 Drawn By: paul_6392	

Sheet 3: Pulse Distribution



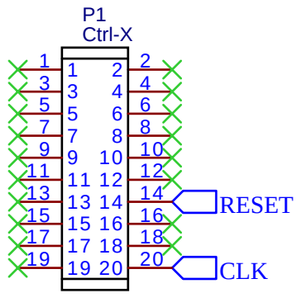


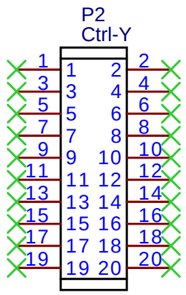
S1-S9, S2'-S12' connect to FSM stages, pulse distribution and indicators (sheet 1 & 2)

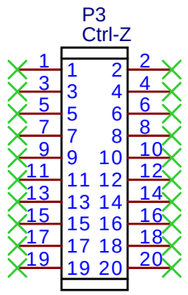
P-A - P-M connect to Pulse bus via upper card interconnect (sheet 4) and indicators (sheet 5)

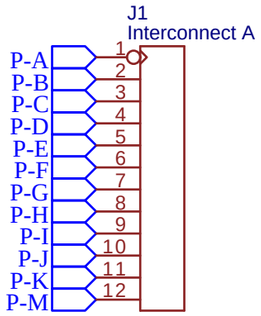
TITLE: Relay Computer : Sequencer Lower Card		REV: 1.1
Relay Computer	Company: Paul Law	Sheet: 3/5
	Date: 2019-09-23 Drawn By: paul_6392	

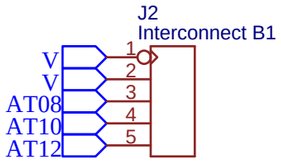
Sheet 4: Backplane & Inter-card connections

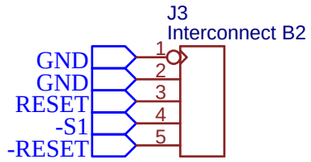


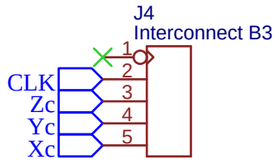












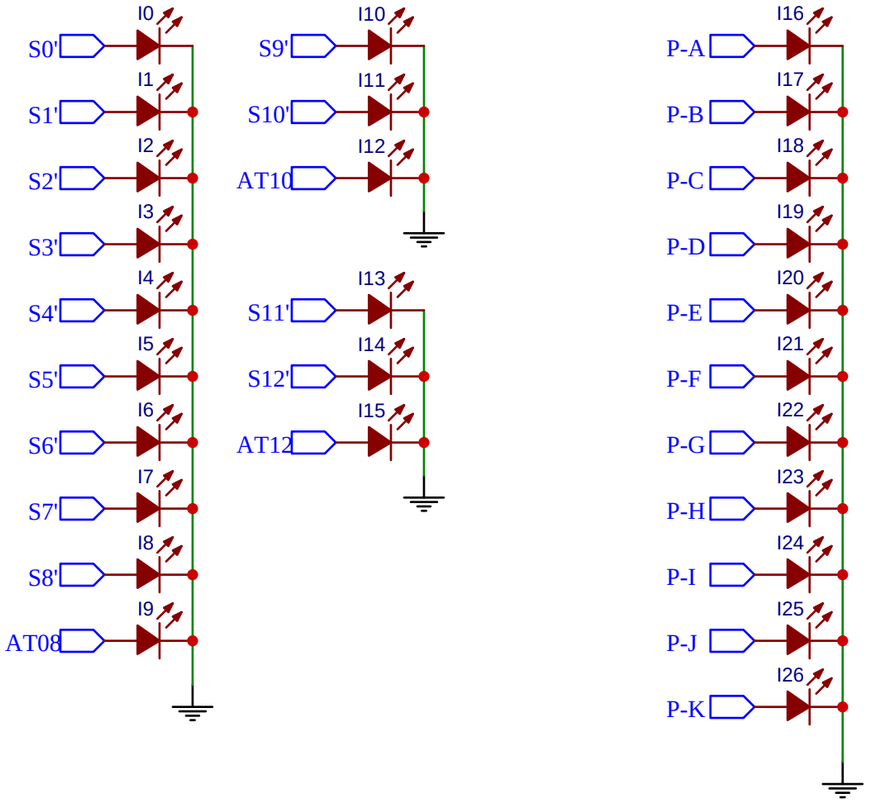
Jumper block A and B is used to map control signals from backplane Ctrl-Y bus

A0-AF signals connect to gating relays (sheet 2)
D0-D7 signals connect to gating relays (sheet 2)

LdH, LdL and LdHL signals connect to control relays (sheet 3)
SelH, SelL and SelHL signals connect to control relays (sheet 3)

TITLE: Relay Computer : Sequencer Lower Card		REV: 1.1
Relay Computer	Company: Paul Law	Sheet: 4/5
	Date: 2019-09-23 Drawn By: paul_6392	

Sheet 5: Card Status LEDs



Important Note: All LEDs shown are 12V type (with integral resistor)

S0'-S12' signals connect to FSM stage relays (sheet 1 & 2)
AT08/AT10/AT12 signals connect to OP bus via upper card interconnect (sheet 4)
P-A thru P-K signals connect to pulse distribution (sheet 3)

TITLE: Relay Computer : Sequencer Lower Card		REV: 1.1
Relay Computer	Company: Paul Law	Sheet: 5/5
	Date: 2019-09-23 Drawn By: paul_6392	