
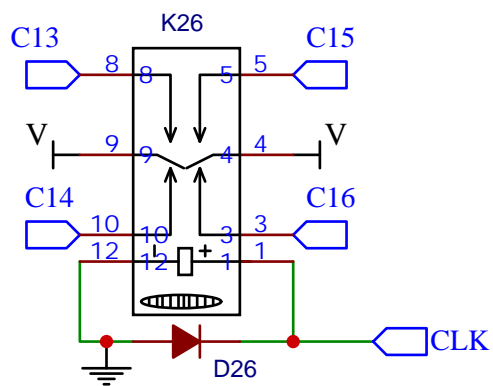


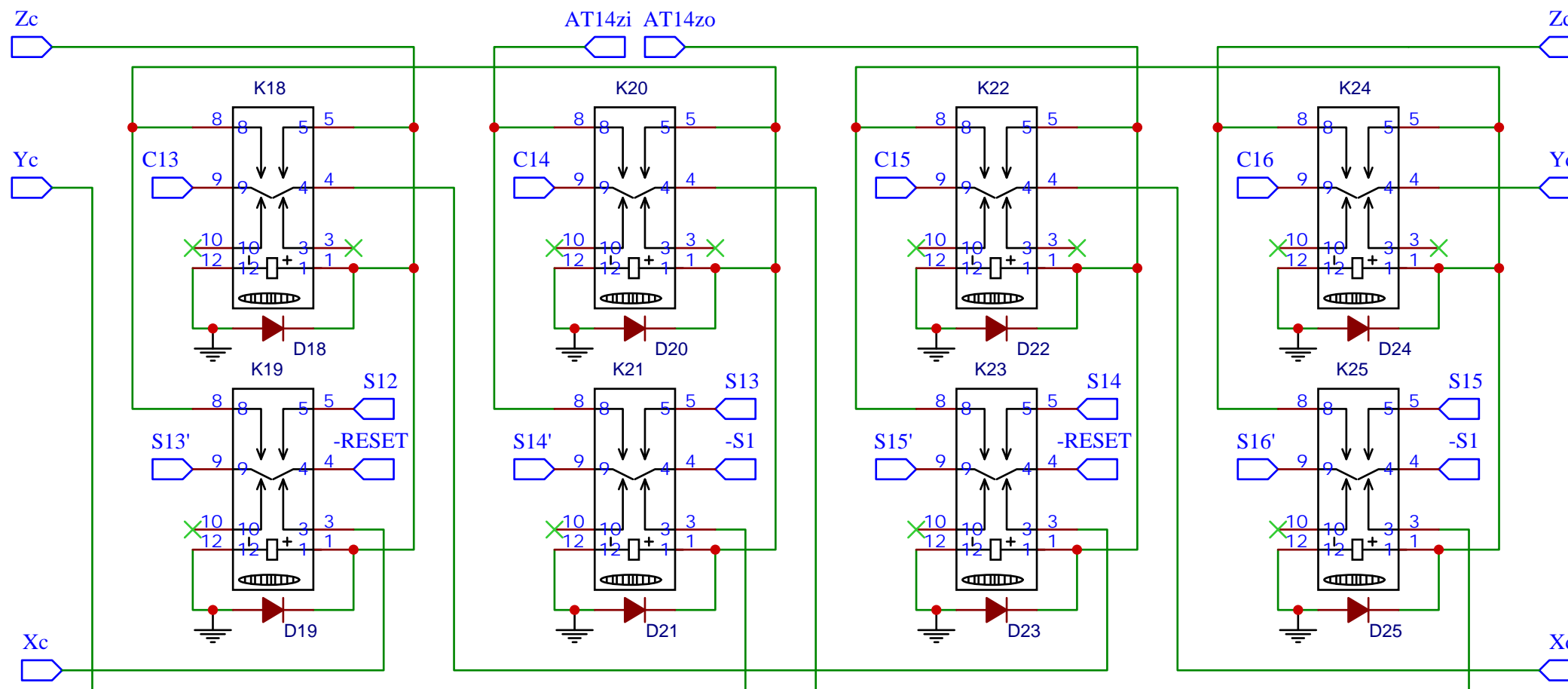
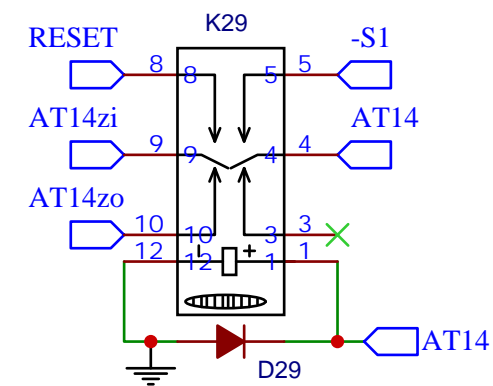
CLK and RESET signals connect to control X bus via lower card connect (sheet 4)
 Xd, Yd, Zd connect from previous FSM stage (sheet 2)
 S16-S23, S17'-S23', ~S1 signals connect to pulse distribution and indicators (sheet 3 & 5)

TITLE: Relay Computer : Sequencer Upper Card		REV: 1.1
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Clock Divider



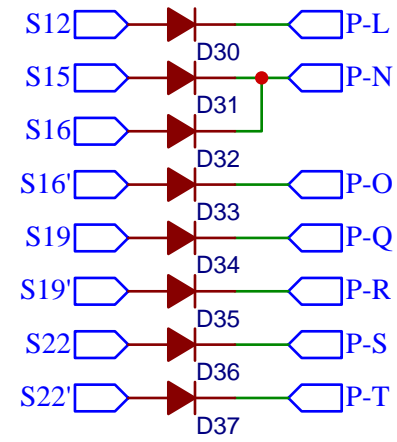
Abort Latch 14




CLK and RESET signals connect to control X bus via lower card connect (sheet 4)
 AT14 signal connects to OP bus (sheet 4)
 Xc, Yc, Zc connect from previous FSM stage via lower card connect (sheet 4)
 Xd, Yd, Zd connect to next FSM stage (sheet 1)
 S12-S15, S13'-S16', ~S1 signals connect to prev FSM stage, pulse dist and indicators (sheet 1, 3 & 5)

TITLE: Relay Computer : Sequencer Upper Card		REV: 1.1
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	Date: 2019-09-23	Drawn By: paul_6392

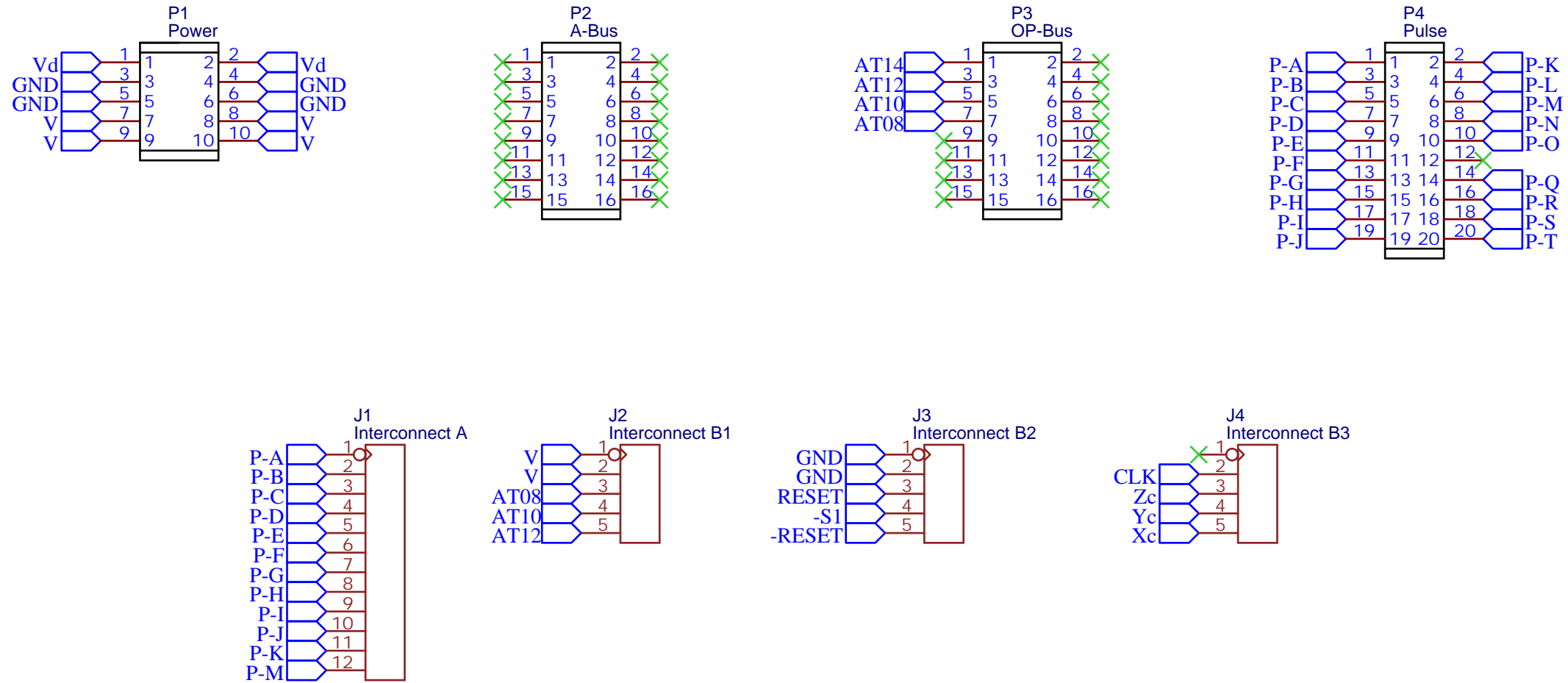
Sheet 3: Pulse Distribution



S12-S22, S16'-S22' connect to FSM stages, pulse distribution and indicators (sheet 1 & 2)
 P-L - P-T connect to Pulse bus (sheet 4) and indicators (sheet 5)

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Sheet 4: Backplane & Inter-card connections




Jumper block A and B is used to map control signals from backplane Ctrl-Y bus

A0-AF signals connect to gating relays (sheet 2)

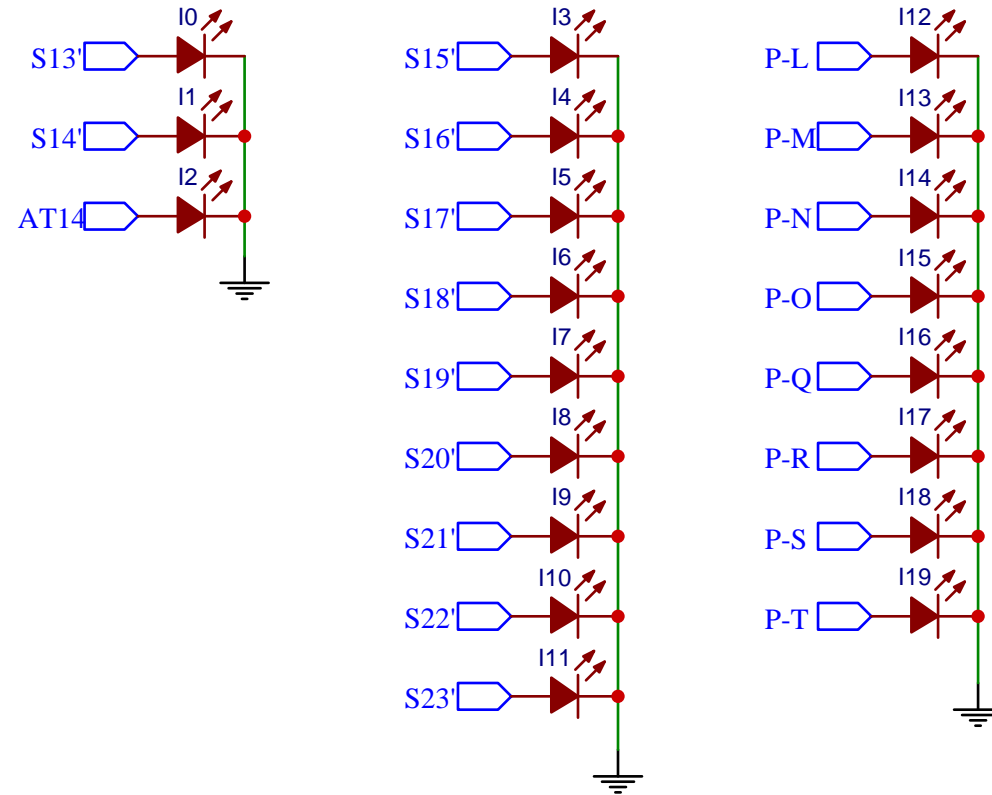
D0-D7 signals connect to gating relays (sheet 2)

LdH, LdL and LdHL signals connect to control relays (sheet 3)

SeIH, SeIL and SeIHL signals connect to control relays (sheet 3)

TITLE: Relay Computer : Sequencer Upper Card		REV: 1.1
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Sheet 5: Card Status LEDs




Important Note: All LEDs shown are 12V type (with integral resistor)

S13'-S23' signals connect to FSM stage relays (sheet 1 & 2)

AT14 signal connect to OP bus (sheet 4)

P-L thru P-T signals connect to pulse distribution (sheet 3)

TITLE: Relay Computer : Sequencer Upper Card		REV: 1.1
	Company: Paul Law	Sheet: 5/5
	Date: 2019-09-23	Drawn By: paul_6392